**DCS LAB **

**Experiment - 5**

**Aim:** Implement 1 to 2, 2 to 4 and 3 to 8 line decoder using dataflow, behavioral and mixed modeling in VHDL. Implement Booleans functions using decoders.

Description:

Part1:

1. Using behavioral architecture, implement a 2 to 4 line decoder.
2. Using dataflow modeling, implement a 3 to 8 line decoder.
3. Implement the following function using a 3 to 8 line decoder by using structural architecture. F(A, B, C) = ∑ (1, 2, 5, 7)
4. Design an entity to encode a 4 bit array of binary number system to the corresponding 4 bit array of gray code. (input and output are STD\_LOGIC\_VECTOR)
5. Implement a 4 to 16 line decoder using only 2 to 4 line decoders, using structural modeling. (input and output are STD\_LOGIC\_VECTOR)

Part2:

1. For each type of the above implementations generate the synthesis report.
2. Study delay, and cell usage for each implementation.
3. Verify using appropriate test benches.